

09/685270 CJC

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor : Eric M. Dowling
 Patent No. : 6,823,505 B1
 Issued : November 23, 2004
 For : **PROCESSOR WITH
 PROGRAMMABLE
 ADDRESSING MODES**



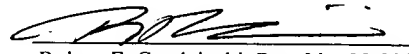
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March 11, 2005

(Date)


 Robert F. Gazdzinski, Reg. No. 39,990

TRANSMITTAL LETTER

Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450
 Attn: Certificate of Correction Branch

Dear Sir:

Enclosed herewith please find the following documents with regard to the above-identified application:

1. Request For Certificate Of Correction Pursuant To 37 C.F.R. § 1.322 and 1.323 (2 pages);
2. Certificates of Correction (3 pages);
3. Check in the amount \$100.00; and
4. Return prepaid postcard.

Certificate
MAR 17 2005

Respectfully submitted, **of Correction**

Dated: 3/11/05

By: 

Robert F. Gazdzinski
 Registration No. 39,990
 11440 West Bernardo Court, Suite 375
 San Diego, CA 92127
 Telephone: (858) 675-1670
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MAR 21 2005



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REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 C.F.R. §§ 1.322 AND 1.323

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
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Dear Sir:

Enclosed for filing is a Certificate of Correction in duplicate in connection with the above-identified patent.

Upon reviewing the above-identified patent, patentee noted several typographical errors which should be corrected. Applicant files this request pursuant to 37 C.F.R. §§ 1.322 and 1.323, as the errors were made by both Applicant, and the United States Patent and Trademark Office.

A check in the amount of \$100.00 is enclosed herewith to cover the filing of a certificate of correction pursuant to 37 C.F.R. § 1.323. The Commissioner is hereby authorized to charge

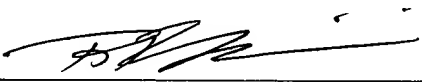
Docket No. : SEARCHP.008DV1
Patent No. : 6,823,505 B1
Issued : November 23, 2004

any deficiency in the fees filed, asserted to be filed or which should have been filed herewith to
Deposit Account No. 501423. A duplicate copy of this paper is enclosed.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

Dated: 3/11/05

By: 

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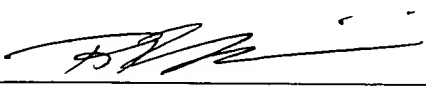
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Dated: 3/11/05

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DATED : November 23, 2004
INVENTOR(S) : Eric M. Dowling

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

First Page (Related U.S. Application Data)

"Division of application No. 09/022,285, filed on Feb. 11, 1998, now Pat. No. 6,163,836."

Should Read:

--**Divisional** of application No. 09/022,285, filed on Feb. 11, 1998, now Pat. No. 6,163,836.--

Column 1, Lines 24-26

"The CICS architectures are being replaced by Reduced Instruction Set Computers (RISC) which are based on a simple load-store architecture. In a load-store architecture,"

Should Read:

--The **CISC** architectures are being replaced by Reduced Instruction Set Computers (RISC) which are based on a simple load-store architecture. In a load-store architecture,--

Column 8, Lines 14-16

"Program data is stored in the data memory 120 and carried by the data bus 112 which interconnects various elements, such as the MAC 116, the register set 102."

Should Read:

--Program data is stored in the data memory 120 and carried by the data bus 112 which interconnects various elements, such as the MAC 116 **and** the register set 102.--

MAILING ADDRESS OF SENDER: Robert F. Gazdzinski
GAZDZINSKI & ASSOCIATES PATENT NO. 6,823,505 B1
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San Diego, CA 92127

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This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Column 12, Lines 25-27

"Table 3 list the code to compute the transpose address using a TMS320C2x to which the programmable AAU 350 has been added, as shown in FIG. 2. The code in Table 3 assumes"

Should Read:

--Table 3 **lists** the code to compute the transpose address using a TMS320C2x to which the programmable AAU 350 has been added, as shown in FIG. 2. The code in Table 3 assumes--

Column 14, Lines 1-2

"500 can provided higher level combinatorial functions not provided by the cross-bar switch. The PLA 500 has sixteen"

Should Read:

--500 can **provide** higher level combinatorial functions not provided by the cross-bar switch. The PLA 500 has sixteen--

Column 17, Lines 14-20 (Claim 1)

"writing a second program in a second programming language, said second program configured to implement a desired algorithm, wherein the second programming language comprises a fixed set instructions that make use of a fixed set of addressing modes, ~~wherein at least one of the addressing modes comprises a user defined addressing mode;~~"

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Column 21, Lines 7-14 (Claim 42)

"a first software module comprising a collection of opcodes assembled from a fixed assembly language that has a fixed set of instructions, a fixed set of fixed addressing modes, and at least one user-defined auto-update addressing mode, wherein the execution of the first software module results in the implement an application algorithm through a sequence of individual op-code executions defined by a program flow; and"

Should Read:

--a first software module comprising a collection of opcodes assembled from a fixed assembly language that has a fixed set of instructions, a fixed set of fixed addressing modes, and at least one user-defined auto-update addressing mode, wherein the execution of the first software module results in the **implementation of** an application algorithm through a sequence of individual op-code executions defined by a program flow; and"

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